Quantum Random Access Memory

Carsten Neumann

26.07.2018

What is a Random Access Memory?

A Random Access Memory (RAM) is used to store information in an array of memory cells. Each of these cells can be addressed at will. It uses the following coponents:

- **Memory array:** Contains information stored in memory cells. Each cell has a unique address
- **Address register:** When the address register is initialized with an address of a memory cell, the information of this cell is returned at the
- **Output register**

What is a Random Access Memory?

Conventional architecture:

- The $N = 2^n$ memory cells are arranged at the end of a bifurcation graph, which consits of n levels.
- If the j-th bit of the address register is 0, then a signal that reached a gate at the j-th level will follow the left route, otherwise the right route.
- At the end, there is a unique path through the graph, which leads to one of the N memory cells.

What is a Random Access Memory?

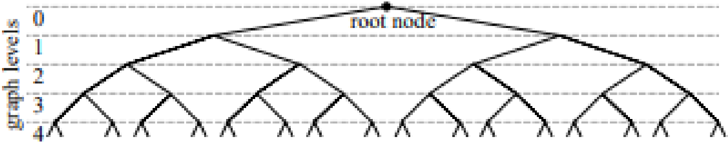

FIG. 1: Bifurcation graph of the RAM addressing.

Now in the quantum realm

- If the address and output registers are composed of qubits, the qRAM can perform memory access in coherent superposition.
- If the address register is in a superposition, the output register will return a superposition of data, correlated with the address register:

$$\sum_j \psi_j \left|j\right\rangle_a \rightarrow \sum_j \psi_j \left|j\right\rangle_a \left|D_j\right\rangle_d$$

Now in the quantum realm

We first look at the conventional archtitecure:

- The j-th qubit of the address register controls all gates of the j-th level
  $\Rightarrow$ We have a superposition of the form

  $$\sum_j |j_0 j_1 \cdots j_{n-1}\rangle_a \otimes |j_0\rangle_{s_0} |j_1\rangle_{s_1}^{\otimes 2} \cdots |j_{n-1}\rangle_{s_{n-1}}^{\otimes 2^{n-1}}$$

  where j_i is the value of the i-th qubit in the address register and s_i the i-th level of the graph. This consists of $O(N)$ quantum gates and is therefore highly susceptible to decoherence.

Now in the quantum realm

- To complete a memory call, a bus qubit is sent through the graph, following the superposition of paths
- The state of the bus qubit is changed according to the information in the memory cell at the end of the paths and is sent back to the root node by the same path
- The bus qubit is now in a superposition of states, correlated to the address register

bucket-brigade architecture

- In the bucket-brigade architecture, the gates in the bifurcation graph are replaced by three-level memory elements (trits). The trits are initialized in the level *wait*. The bits of the address register are sent one after the other through the graph.
  - If the trit is in the level *wait*, its value will be changed according to the value of the incoming bit: if the value is 0, the trits level gets changed to *left*, if it is 1, the level gets changed to *right*
  - If the trit is in the level *left* or *right*, any incoming bit will take the left respectively the right path
- After all the bits of the address register passed through the graph, a bus signal is sent through the graph to the memory cell the address register was pointing to
- The bus signal gets sent back. Everytime the signal encounters a trit, the trits value is reset to *wait*

bucket-brigade architecture in the quantum realm

- We have quantum gates with the three states $|left\rangle, |right\rangle$ and $|wait\rangle$ (qutrits)
- When a qubit reaches a qutrit in the state $|wait\rangle$, the qutrits state changes according to

$$U|0\rangle|wait\rangle \to |f\rangle|left\rangle, U|1\rangle|wait\rangle \to |f\rangle|right\rangle$$

- After all qubits of the address register are sent through the graph, we have a superposition of paths

$$\sum_j \psi_j |j_0\rangle_{t_0} |j_1\rangle_{t_1(j_0)} \cdots |j_{n-1}\rangle_{t_{n-1}(j_{n-2})} \otimes_{l_j} |wait\rangle_{t_{l_j}}$$

where $t_i(j_{i-1})$ is the qutrit which is aimed by the qutrit of the level before

benefits of the bucket-brigade architecture

- Only $O(r \log N)$ operations are needed, if the address register is in a superposition of r states, opposed to $O(N)$ in the conventional architecture. In algorithms where r is small, this is a huge improvement
- If in the conventional architecture only one gate is decohered, the fidelity of the state is in average reduced by $1/2$.
  If in the bucket-brigade architecture a fraction ϵ of qutrits is decohered, the fidelity of the state is in average $O(1 - \epsilon \log N)$, when all qutrits are involved in the superposition

Possible implementation

- The qutrits are composed by trapped atoms or ions with ground state $|wait\rangle$ and two excited states $|left\rangle$ and $|right\rangle$
- The address and bus qubits are photons
- A photon in the polarization state $|0\rangle$ leads to a $|wait\rangle \rightarrow |left\rangle$ transition, a photon in the state $|1\rangle$ to a $|wait\rangle \rightarrow |right\rangle$ transition
- Strong classical pulses are used to couple the three states of the atom with extra energy levels
- If a photon reaches an atom in the $|left\rangle$-state, there is a cyclic transition into a higher $|left'\rangle$-state. After the retransition into the $|left\rangle$-state, the photon is re-emmited in the left direction
- At the end, the transition into the $|wait\rangle$-state is induced by classical pulses. Photons are emitted according to the state the qutrits were in before the transition

Possible implementation

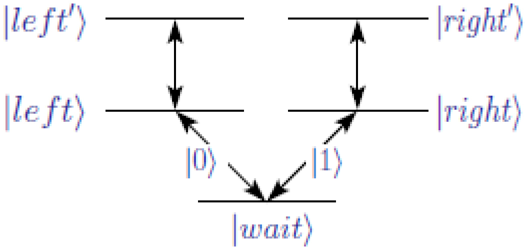

Figure: The qutrit